

A detailed cross-sectional view of a semiconductor device assembly. The assembly consists of a substrate (1) with a central opening (12). A central layer (2) is positioned above the opening, with a central region (4) and side regions (11). A layer (9) is on top of the central region (4), with a central part (10) and side parts (13, 14). A layer (16) is on top of the side parts (13, 14). A layer (3) is on top of the central region (4) and side parts (13, 14). A layer (8) is on top of the central region (4) and side parts (13, 14). A layer (7) is on top of the central region (4) and side parts (13, 14). A layer (5) is on top of the central region (4) and side parts (13, 14). A layer (6) is on top of the central region (4) and side parts (13, 14).

A cross-sectional view of a multi-layered structure. It consists of a top layer (9) with diagonal hatching, a middle layer (10) with horizontal hatching, and a bottom layer (11) with diagonal hatching. A central rectangular feature (12) is embedded in the bottom layer, with a smaller rectangular feature (13) on top of it. A layer (14) is positioned between the middle layer (10) and the bottom layer (11) on the sides of the central feature.

FIG.3

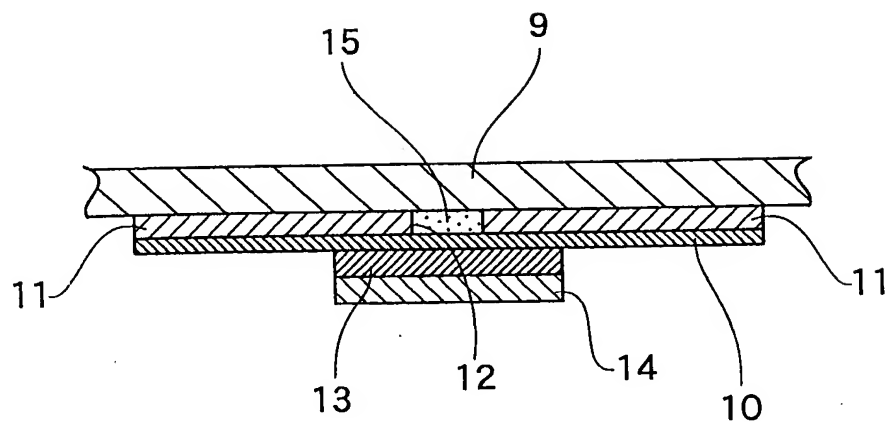


FIG.4

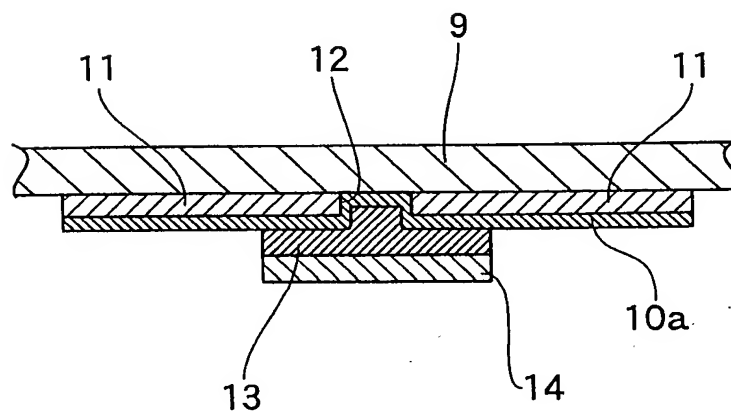


FIG.5

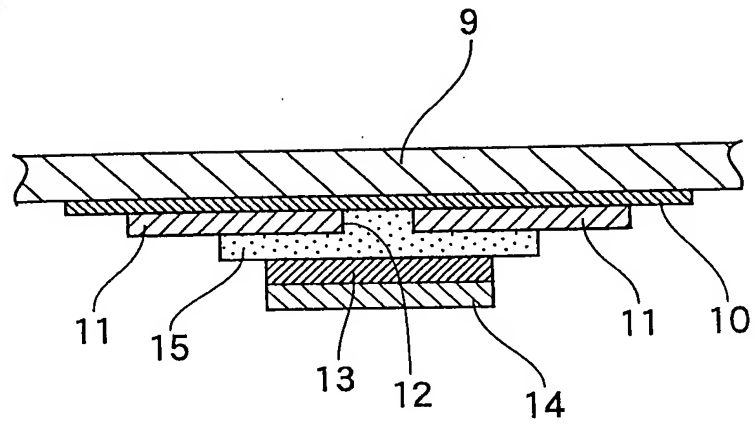


FIG.6

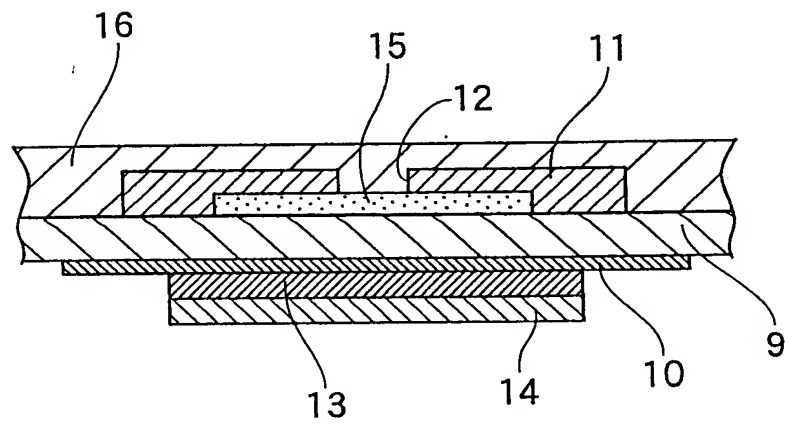


FIG.7

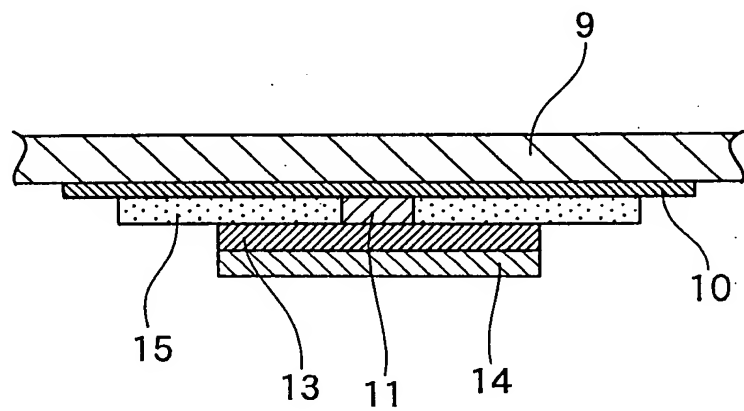


FIG.8

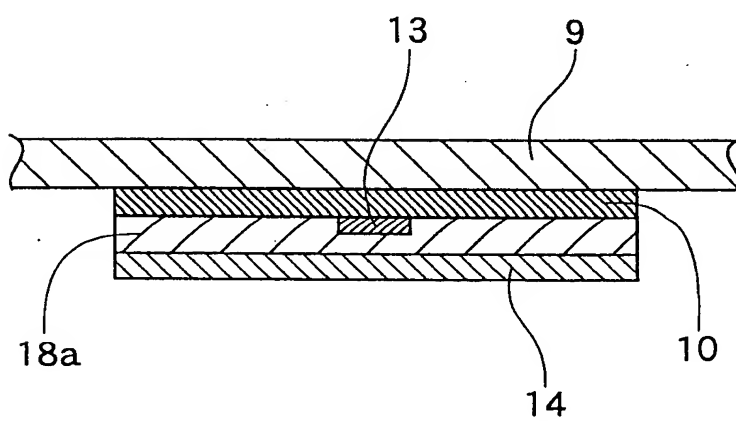


FIG.9

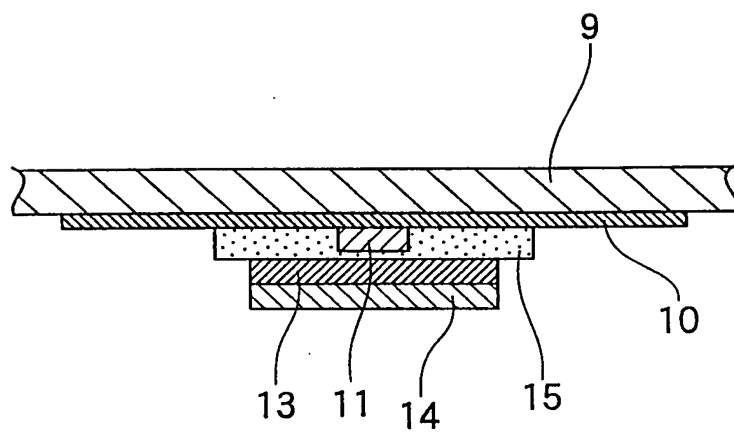


FIG.10

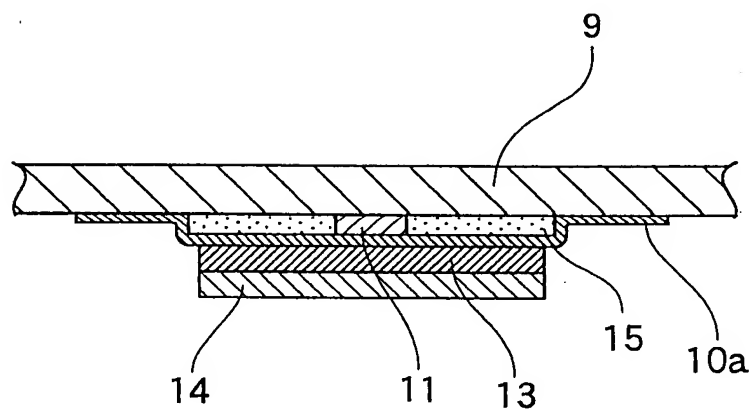


FIG.11

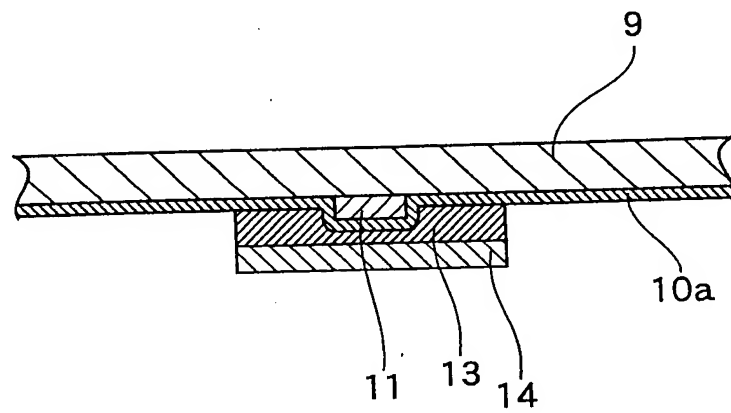


FIG.12

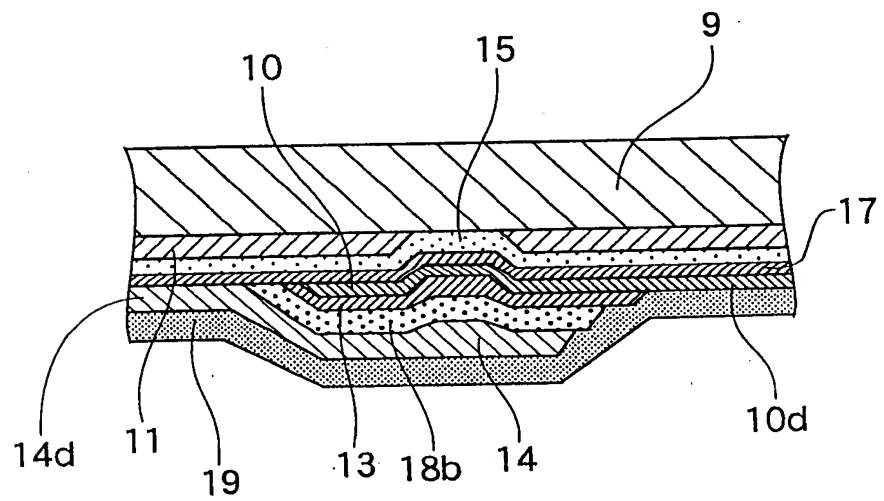


FIG.13

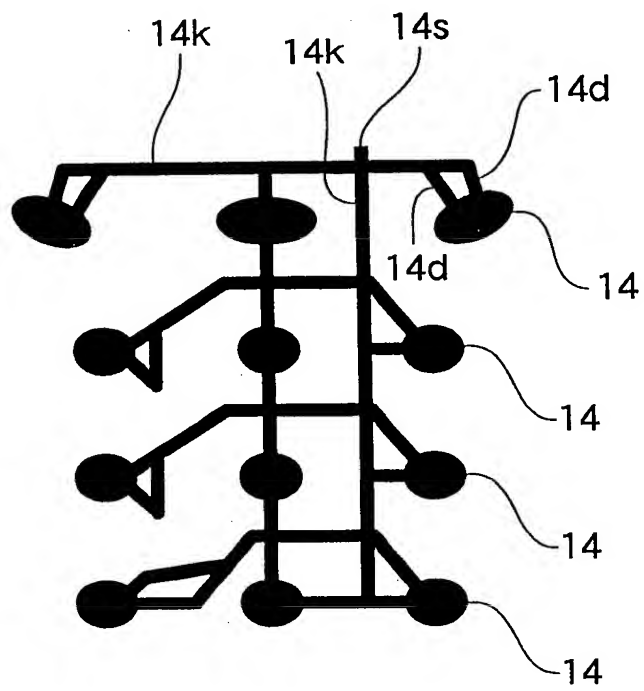


FIG.14

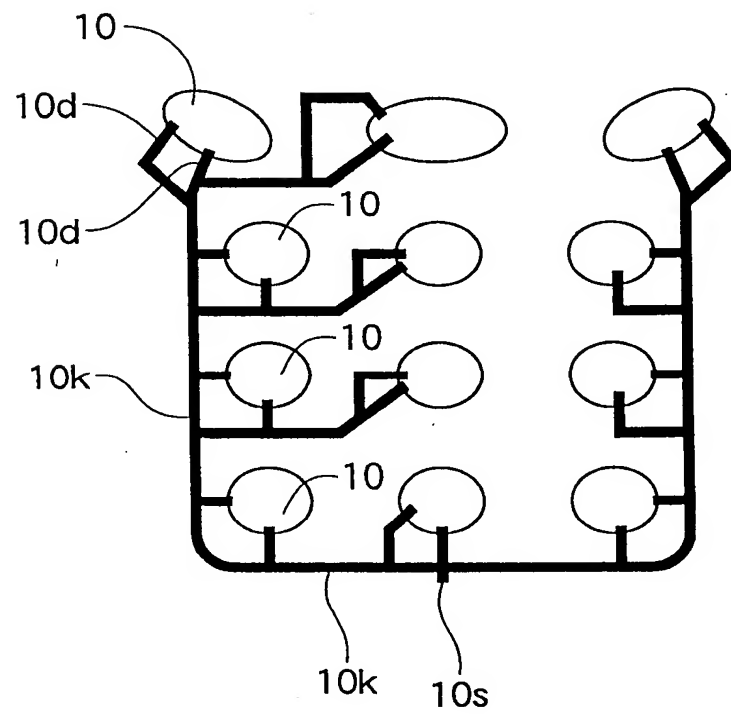


FIG.15

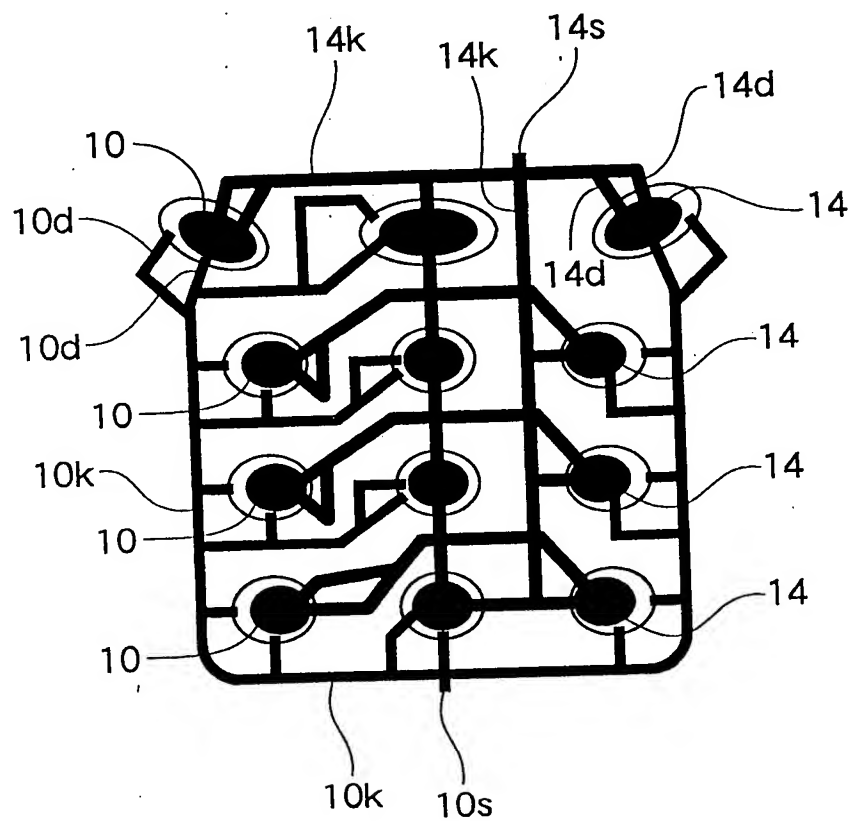


FIG.16

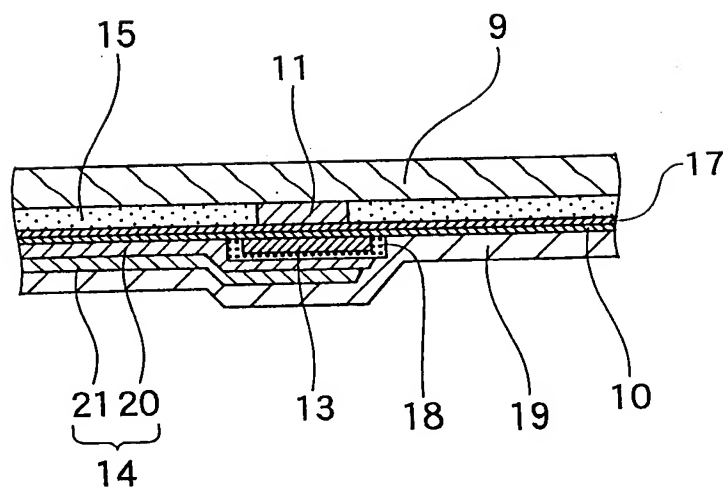




FIG.17

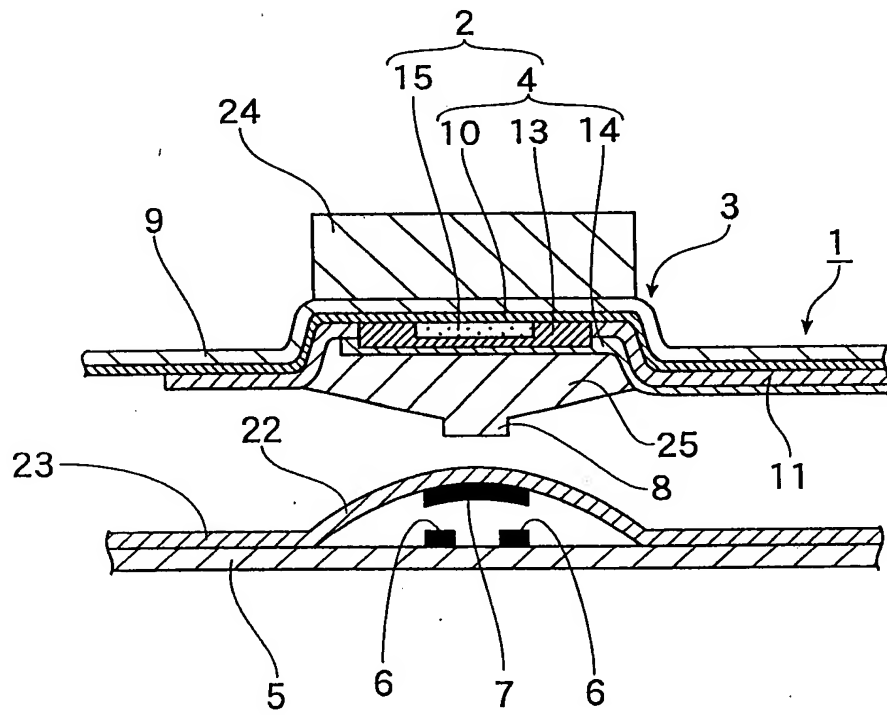


FIG.18

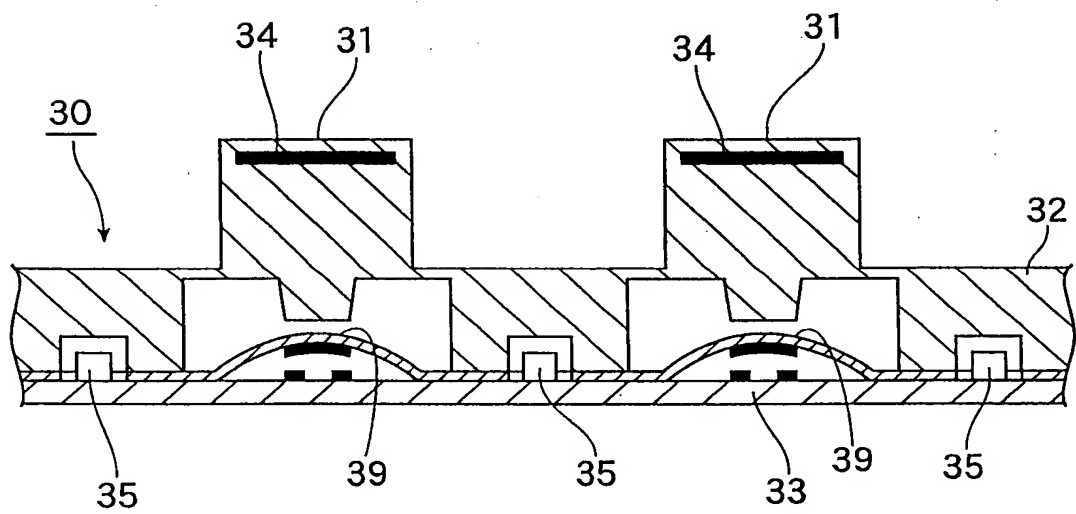


FIG.19

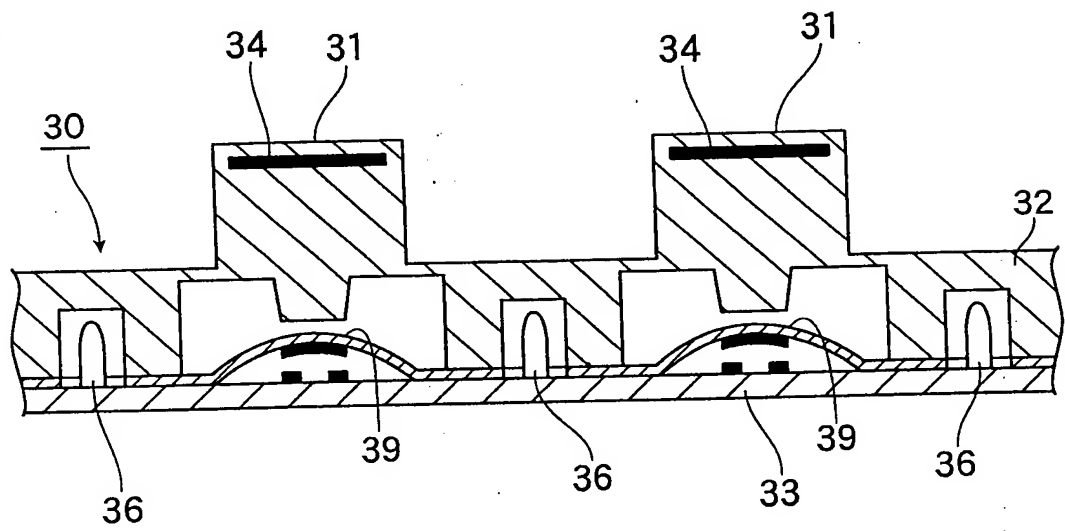


FIG.20

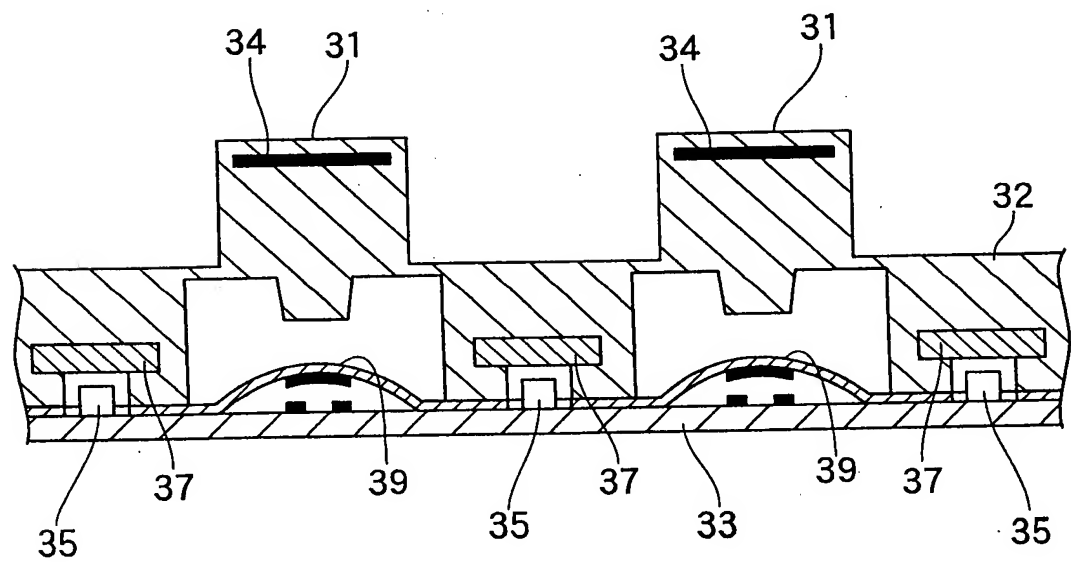


FIG.21

